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10/689,298	10/20/2003	Tommy Hsiao	184-P065D1C1	4293

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,298	HSIAO ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 17-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9 and 17-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1-26-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 3 – 9, 17 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

a. With regard to claim 1, it is not clear where in the originally filed parent specification support for "the drain implant being provided only in the substrate adjacent to the second edge of each of the plurality of gate stacks" [emphasis added] can be found.

b. With regard to claim 19, it is not clear where in the originally filed parent specification support for "performing a drain implant only adjacent to the second edge of the stacked gate" [emphasis added] can be found. Further, it is not clear where in the originally filed parent specification support for "limiting the duration and temperature of subsequent heat treatments of the semiconductor memory to reduce diffusion of the drain implant" can be found

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 19 – 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 19, it is not clear how "limiting the duration and temperature of subsequent heat treatments of the semiconductor memory to reduce diffusion of the drain implant" is performed. There is no standard expressed in the claims or the specification that can be compared to and thus quantify the "limiting" step. How are the duration and temperature of subsequent heat treatment limited?

With regard to claims 24 and 25, how can a rapid thermal anneal be performed while still "limiting subsequent heat treatments"?

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3 – 5, 7 – 9, 17, 18, 19 – 21, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (USPAT 5482881, Chen) in view of Gardner et al. (USPAT 5953613, Gardner).

With regard to claim 1, Chen discloses in figures 3 and 6 a method for providing a semiconductor memory device including a substrate (116) and at least one field isolation region (300). Chen discloses in figures 3 and 6 providing (450) a plurality of gate stacks (700) above the substrate, each of the plurality of gate stacks including a first edge and a second edge, each of the plurality of gate stacks crossing the at least one field isolation region (300). Chen discloses in figures 3, 6 – 6c, and 6f providing a source implant (458/670, DDI/MDDI, 112) adjacent to the first edge of each of the plurality of gate stacks. Chen discloses in figures 3, 6, and 6d driving (462) the source implant under the first edge of each of the plurality of gate stacks. Chen discloses in figures 3, 6, 6e, and 6f providing a drain implant (672, MDD2, 114,) after, the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks. Chen does not disclose providing the drain implant only in the substrate adjacent the second edge of each of the plurality of gate stacks. Gardner discloses in figure 1a and the abstract providing a drain implant (20), the drain implant being provided only in a substrate (12) adjacent to a second edge of a gate stack (13/14). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the drain implant of Gardner only adjacent one side of the gate stacks in the method of Chen in order to improve subthreshold characteristics and punchthrough behavior of the devices as stated by Gardner in the abstract.

With regard to claim 3, Chen discloses in figures 3 and 6 – 6f wherein the source implant providing step includes the step of providing a first source implant (DDI) and a second source implant (MDD1) adjacent to the first edge of each of the plurality of gate stacks. Chen discloses in figures 3 and 6 – 6f wherein the driving step includes the step of driving the first source implant and the second source implant under the first edge of each of the plurality of gate stacks.

With regard to claim 4, Chen discloses in figures 3, 6, 6b – 6d, and 6f further comprising the step of providing a first spacer and a second spacer (both formed of insulating layer 720) for each of the plurality of gate stacks, the first spacer being disposed along the first edge of each of the plurality of gate stacks, the second spacer being disposed along the second edge of each of the plurality of gate stacks.

With regard to claim 5, Chen discloses in figures 3 and 6 – 6a further comprising the step of providing a self-aligned source etch (454).

With regard to claim 7, Gardner teaches in column 7, lines 29 – 39 wherein the drain implant is As (arsenic).

With regard to claim 8, Chen discloses in figures 3 and 6 – 6f and column 8, lines 19 – 52 wherein the second source implant is As.

With regard to claim 9, Chen discloses in figure 6 oxidizing after the drain implant has been provided. It is not clear if Chen further teaches comprising the step of providing a rapid thermal anneal after the drain implant has been provided. Gardner further teaches in column 7, lines 49 – 52 comprising a step of providing a rapid thermal anneal after a drain implant has been provided. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the rapid thermal annealing step of Gardner in the method of Chen and Gardner in order to activate the drain dopants and remove crystalline damage as taught by Gardner in column 7, lines 49 – 52.

With regard to claim 17, Chen discloses in figures 3, 6, and 6d wherein the step of driving the source implant under the first edge of each of the plurality of gate stacks comprises a thermal treatment (462).

With regard to claim 19, Chen discloses in figures 3 and 6 – 6f forming a gate stack. Chen discloses in figures 3 and 6 – 6f performing a source implant adjacent to a first edge of the stacked gate. Chen discloses in figures 3 and 6 – 6f heat treating the semiconductor memory so that the source implant diffuses under the first edge of the stacked gate. Chen discloses in figures 3 and 6 – 6f performing a drain implant adjacent to a second edge of the stacked gate. Chen does not disclose providing the drain implant only in the substrate adjacent the second edge of the gate stack. Gardner discloses in figure 1a and the abstract providing a drain implant (20), the drain implant being provided only in a substrate (12) adjacent to a second edge of a gate stack (13/14). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the drain implant only adjacent one side of the gate stack of Gardner in the method of Chen in order to improve subthreshold characteristics and punchthrough behavior of the device as stated by Gardner in the abstract. Chen discloses in figures 3 and 6 – 6f limiting duration and temperature subsequent heat treatment of the semiconductor memory to reduce diffusion of the drain implant, so that the source implant extends further under the first edge of the stacked gate than the drain implant extends under the second edge of the stacked gate. It should be noted that the "limiting duration" limitation is met by Chen because Chen clearly discloses the claimed results of this step in figure 6f.

With regard to claim 20, Chen discloses in figures 3 and 6 – 6f wherein performing the source implant comprises performing a double diffused implant (DDI).

With regard to claim 21, Chen discloses in figures 3 and 6 – 6f wherein performing the source implant comprises performing a double diffused implant (DDI), and performing a moderately doped drain implant (MDDI).

With regard to claim 24, Chen discloses in figure 6 oxidizing after the drain implant has been provided. It is not clear if Chen further teaches comprising the step of providing a rapid thermal anneal after the drain implant has been provided. Gardner further teaches in column 7, lines 49 – 52 comprising a step of providing a rapid thermal anneal after a drain implant has been provided. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the rapid thermal annealing step of Gardner in the method of Chen and Gardner in order to activate the drain dopants and remove crystalline damage as taught by Gardner in column 7, lines 49 – 52.

With regard to claim 25, Gardner teaches in column 7, lines 48 – 52 where a rapid thermal anneal comprises heat treating a semiconductor memory in a furnace at a temperature of about 1000 degrees Celsius for about 10 seconds.

5. Claims 6 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Gardner as applied to claims 1, 4, and 19 above, and further in view of Miyata (USPAT 5183773).

Chen discloses in figures 3 and 6 – 6f the semiconductor memory device and spacers. It is not clear if Chen and Gardner teach wherein the semiconductor memory device further includes a periphery including a plurality of logic devices and wherein the spacer-providing step further includes the step of providing the first spacer and the second spacer concurrently with a plurality of spacers in the periphery of the semiconductor memory device. Miyata teaches in figures 3l – 3m wherein a semiconductor memory device (32) further includes a periphery (34 and 36) including a plurality of logic devices (33 and 35) and wherein a spacer (98) providing

step further includes the step of providing a first spacer and a second spacer concurrently with a plurality of spacers in the periphery of the semiconductor memory device. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the peripheral logic devices and concurrent spacer forming step of Miyata in the method of Chen and Gardner in order to save space on a mother board and therefore reduce costs of fabrication by further consolidating fabrication steps.

6. Claims 22 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Gardner as applied to claim 19 above, and further in view of Shah et al. (USPAT 5065208, Shah).

Chen discloses in column 6, lines 64 – 67 wherein heat treating the semiconductor memory comprises annealing the semiconductor memory at a temperature of 1050 degrees Fahrenheit. Chen and Gardner do not teach annealing at 900 degrees Celsius for about 40 minutes. Shah teaches in column 10, lines 33 – 37 wherein heat treating a semiconductor memory comprises annealing the semiconductor memory in a furnace at about 900 degrees Celsius for about 40 minutes. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the annealing of Shah in the method of Chen and Gardner in order to drive an N type impurity of a source region under gate oxide as taught by Shah in column 10, lines 33 – 37.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1, 3, 4, 6 – 9, 17 – 19, and 24 – 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 5 of U.S. Patent No. 6,235,584 in view of Gardner.

As far as the examiner can ascertain the subject matter of claims 1 and 19 of the application are covered by claim 1 of the patent in view of Gardner, similar to the above 103 rejections using Gardner. The subject matter of claim 3 of the application is covered by claims 1 and 2 of the patent. The subject matter of claim 4 of the application is covered by claim 1 of the patent. The subject matter of claims 6 and 26 of the application are covered by claims 1 and 3 of the patent. The subject matter of claim 7 of the application is covered by claims 1 and 4 of the patent. The subject matter of claim 8 of the application is covered by claims 1 – 5 of the patent in view of Gardner. The subject matter of claims 9, 24, and 25 of the application is covered by

claims 1 – 5 of the patent in view of Gardner. The subject matter of claims 17 and 18 of the application are covered by claims 1 and 2 of the patent.

7. Claim 5, 20, 21 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 5 of U.S. Patent No. 6,235,584 and Gardner and further in view of Chen. It would have been obvious to have the additional features of a self-aligned source etch, DDI implant, and MDDI implant of Chen in the invention of U.S. Patent No. 6,235,584 and Gardner in order to make a working device.

8. Claim 22 and 23 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 5 of U.S. Patent No. 6,235,584 and Gardner and further in view of Shah. It would have been obvious to have the feature of annealing the semiconductor memory in a furnace at about 900 degrees Celsius for about 40 minutes of Shah for the heat treatment in the invention of U.S. Patent No. 6,235,584 and Gardner in order to drive an N type impurity of a source region under gate oxide.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II